AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 6 with the following amended paragraph:

Communication networks, in particular communication networks on integrated circuits, have numerous paths carrying signals from one device to other devices. Multiple paths that are placed near one another can lead to problems related to coupling and capacitative interference. The situation becomes more problematic when multiple paths carrying signals ~~switch~~ switching in the same direction run parallel to a single path switching in the opposite direction.

Please replace the paragraph beginning at page 3, line 25 with the following amended paragraph:

Digital signals[[,]] rise from a zero value to a set value that correlates to a digital value of "1." There is a slight rise time and an associated rising edge, as well as a slight fall time and ~~an~~ a falling edge associated with the transmitted signal. When a signal is transitioning during a rise or fall time, the signal is said to be switching.

Please replace the paragraph beginning at page 4, line 3 with the following amended paragraph:

This invention provides for a delay between signals, specifically signals that are close to one another that are switching in opposite ~~signals~~ directions. While a signal is switching, an adjacent signal is delayed while the transmitting signal completes switching. To determine which signal is delayed, signals are given priorities as to which signal is allowed to switch and which signal is delayed. The delay places the signals out of phase with one another, to allow signals to be transmitted with minimal coupling and capacitance effects from opposite switching signals. Reducing or

eliminating the coupling and capacitance effects allows signal paths to be placed closer to one another.

Please replace the paragraph beginning at page 4, line 24 with the following amended paragraph:

Figure 2 is a block diagram illustrating a network layout with ~~using~~ PDICs and wires. A cell 200 contains PDICs 100, 105, and 110. In certain applications, cell 200 can be part of a larger integrated circuit or system. Cell 200 is ~~consider~~ considered a subsystem that includes PDICs 100, 105, and 110 interconnected to one another, and setting priority as to signal transmission. PDICs 100, 105, 110 act as drivers to transmit signals. PDIC 100 transmits signals along a path 205. PDIC 105 transmits signals along a path 210. PDIC 110 transmits signals along a path 215. Signal paths that are relatively longer in length can require priority over all other paths. For example path 210 can be a longer path, therefore path 210 is given the highest priority of 0. Path 210 can also be a victim path to paths 205 and 215, therefore path 210 is given priority of 0. Priority delay logic within PDICs 100, 105, and 110 allow paths 205, 210, and 215 to be placed relatively close to one another and avoid coupling effects in signal transmission. Allowing the signals to be placed closer to one another provides for a denser architecture and smaller sized circuits.

Please replace the paragraph beginning at page 5, line 6 with the following amended paragraph:

Figure 3 is a block diagram illustrating a network architecture incorporating disable logic signals. This embodiment of the invention provides for PDICs 100, 105, and 110 to act as drivers driving particular signals. PDIC 100 drives a signal A 300. PDIC 105 drives a signal B 305. PDIC 110 drives a signal C 310. PDIC 105 and signal B 305 have priority of 0. Whenever signal B 305 is switched, PDIC 105 provides a disable

signal D0 315 to PDIC 100, and a disable signal D0 320 to PDIC 110. Delaying switching of signal A 300 and signal C 310, allows signal C 305 to be transmitted without interference. Once signal C 305 is switched, delay signal D0 315 and delay signal D0 320 are ~~disable~~ disabled. Hardware, firmware, and/or software logic can provide delay signals. For example, a shot flip-flop device can provide a hardware delay sufficient for switching to occur. Since rise and fall times are known and/or can be accurately estimated, the necessary time delay can be provided that accounts for the rise and fall times.

Please replace the paragraph beginning at page 6, line 25 with the following amended paragraph:

Figure 6 is a timing diagram illustrating multiple priority 0 signals and disabling a priority 1 signal. When two priority 0 signals switch at or near the same time, a disable signal is provided to a common PDIC that is adjacent to the priority 0 signals. In this example, signals B 500 and D 600 are a priority 0 signals, and a disable pulse is sent to common adjacent priority 1 PDIC C 110. Signal D 600 is a signal with relative threshold values V1 605 and V2 610. Signal [[B]] D 600 has a rising edge that begins at time-voltage value 607 and ends at time-voltage value 612. Signal [[B]] D 600 has a falling edge that begins at time-voltage value ~~517~~ 617 and ends at time-voltage value ~~515~~ 615. The rising edge of signal D 600 is represented by the time period D1r 650. The falling edge of signal D 600 is represented by time period D1f 630. Time period D0r 550 has some overlap with time period D1r 650. D0r 550 begins and ends before D1r 650. D0f 555 and D1f 630 also overlap in this example. D0f 555 in this particular case begins and ends before D1f 630. In other cases the time periods may or may not overlap. Overlap depends when the signals are transmitted. Disable signal D01 660 is activated and sent to PDIC 100 during the overlap of rising and falling edges of signal B 500 and signal D 600. An activated disable signal D01 660 is represented by a disable

pulse 675 and a disable pulse 680. Time period Dcr 665 represents the time period overlap of the rising edges of signal B 500 and signal D 600. Time period Dcf 670 represents the time period overlap of the falling edges of signal B 500 and signal D 600. PDIC 100 is disabled from transmitting during the time periods Dcr 665 and Dcf 670.